

PATENT NUMBER ~~2~~

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U.S. UTILITY Patent Application

PATENT DATE

Q.A

CONT/PRIOR

CLASS

SUBCLASS

ART UNIT

EXAMINER

Sharon
0205021

SECRET

70.8

24

2123

Circuit-level memory and combinational block modeling

PTO-2040
12/99

| ISSUING CLASSIFICATION | | | | | | | | | |
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| ORIGINAL | | | | CROSS REFERENCE(S) | | | | | |
| CLASS | | SUBCLASS | | CLASS | SUBCLASS (ONE SUBCLASS PER BLOCK) | | | | |
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| INTERNATIONAL CLASSIFICATION | | | | | | | | | |
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☐ **TERMINAL
DISCLAIMER**

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| Sheets Drwg. | Figs. Drwg. | Print Fig. |
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| Total Claims | Print Claim for O.G. |
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(Assistant Examiner) (Date)

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